

CLAIMS

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What is claimed is:

1. A partially fabricated wafer, comprising:
at least one probe pad;
400 multiple test structures which are selectably multiplexed to said
probe pad in dependence on the voltage applied thereto.
2. The wafer of Claim 1, wherein said probe pad is located in a
scribeline, and occupies more than half the width of said
405 scribeline.
3. The wafer of Claim 1, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
voltage applied to said probe pad.
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4. The wafer of Claim 1, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
sequence of voltages applied to said probe pad.

415 5. A partially fabricated wafer, comprising:
at least one probe pad;
multiple test structures which are all physically close to said probe
pad, and which are selectably multiplexed to said probe pad
in dependence on at least one global input.

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6. The wafer of Claim 5, wherein said probe pad is located in a
scribeline, and occupies more than half the width of said
scribeline.

425 7. The wafer of Claim 5, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
voltage applied to said probe pad.

430 8. The wafer of Claim 5, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
sequence of voltages applied to said probe pad.

said multiple test structures.

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